

HL1361BRxx

DFB Laser Diode Chip Bar

Sample Categories and Disclaimer

Functional sample that has the suffix of “-F” or “-Fx” to the product number is a sample that is designed according to the customer’s request. The purpose of this sample is to check and confirm the product feasibility. Thus the sample may be an R&D prototype or may be a modified current product. This sample may not be manufactured in qualified production lines nor using qualified parts. Basically Oclaro guarantees the requested performance of BOL (Beginning Of Life). Any qualification will not be applied.

Working sample that has the suffix of “-W” or “-Wx” to the product number is a sample to evaluate, confirm and finalize the product specifications. Basically Oclaro guarantees the performance of BOL (Beginning Of Life). Not all qualifications may be completed. This sample may not be manufactured in qualified production lines nor be using qualified components. Until Oclaro Inc. releases the products for general sales, Oclaro Inc. reserves the right to change prices, features, functions, specifications, capabilities and release schedule.

DESCRIPTION

General

The HL1361BRxx is a Distributed Feed-Back (DFB) laser diode chip bar. Front facet and rear facet of each bar are coated by AR (Anti Reflection) and HR (High Reflection) film respectively. One bar contains 34pcs or 35 pcs of LD chips in line. The bar will be shipped as is without electric tests and without visual check for chips. The optical/electrical performances are verified as a wafer verification test. Individual chip is designed for 10Gbit/s operation and for use in the dry N2 hermetic sealed package.

PN information

PN	PN (initial samples)	Chip qty in a bar	Wavelength** (nm)
HL1361BRxx	HL1361BRxx-F	34 or 35	1310

**“xx” are customer code and will be assigned separately.

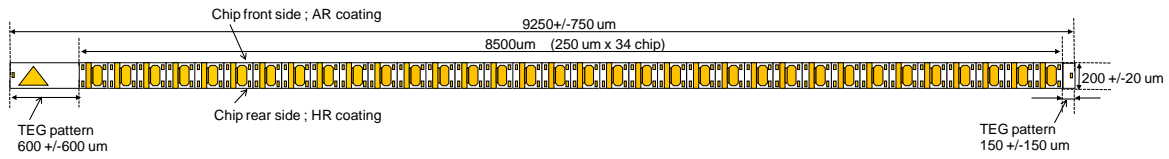
* Actual wavelength range is specified separately.

Outline

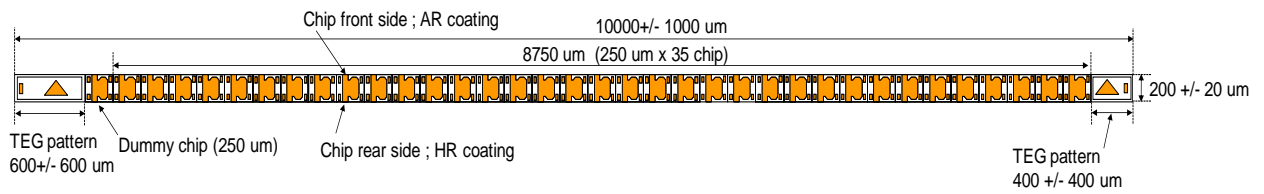
Bar Dimension

The bar will be either Type A or Type B.

Type A



Type B



Pin Configurations



Fig.2 Block Diagram (one LD chip)

Table 1. Pin Configurations

Pin #	Description	Remarks
1	Laser anode (P electrode)	
2	Laser cathode (N electrode)	

MECHANICAL DIMENSIONS

Individual chip size is 250 μm x 200 μm x 92 μm. Fig. 3-5 shows a chip outline and metallization pattern. The Anode has typ. 0.55μm Au film and Cathode has typ. 0.57μm Au film respectively.

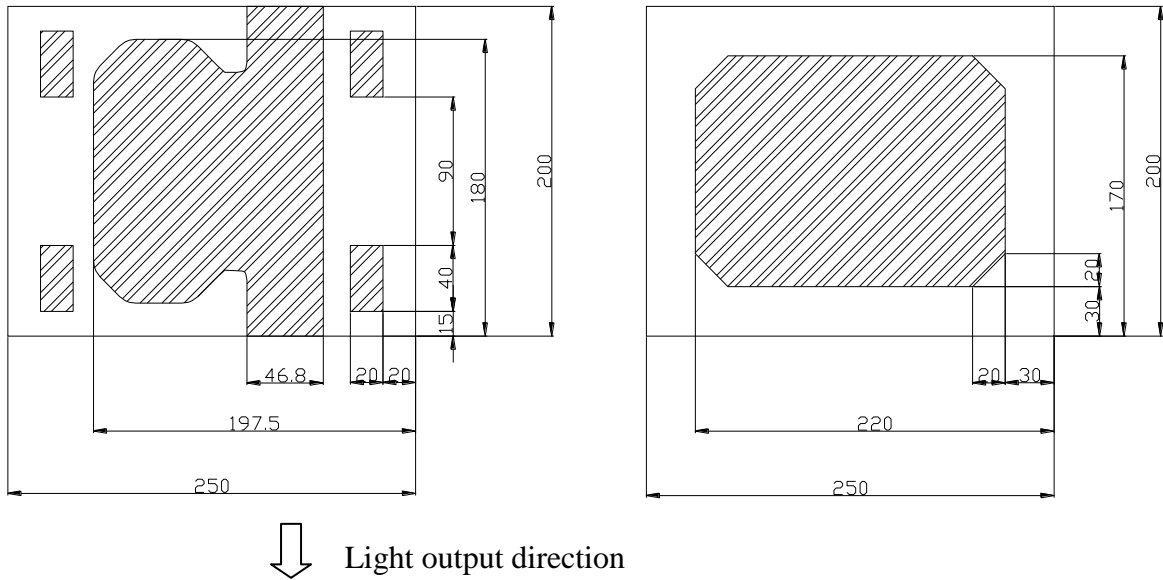


Fig.3 Top view (Anode)

Fig.4 Bottom view (Cathode)

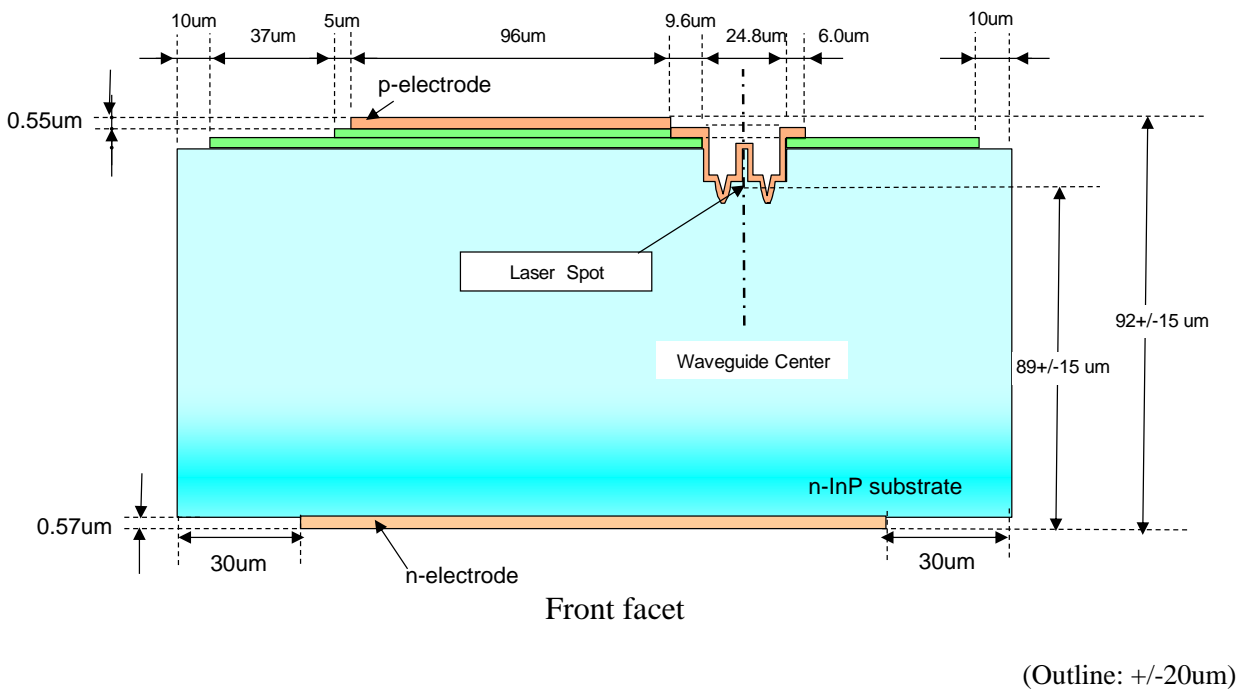


Fig. 5 Chip Outline and Dimensions

PERFORMANCE SPECIFICATIONS

Absolute Maximum Ratings

Since the HL1361BRxx is a bar form, the performance will depend on not only chip performance but also its assembling process including dicing. If the chip is assembled in a proper way, the performance described in Table 2 can be expected but these are not guaranteed values. Oclaro assumes no responsibility for those reliability when they are assembled and/or tested in customer Tc means submount temperature when the chip mounted on Oclaro standard sub-mount soldered on heat sink.

Table 2. Absolute Maximum Ratings (Tc=25°C, unless otherwise specified)

	Absolute Maximum Rating	Min	Max	Unit	
1	Storage temperature	-40	85	C	
2	Operating temperature	-40	95	C	
3	Laser forward bias current	-	150	mA	
4	Laser reverse bias voltage	-	2	V	
5	Die binding temperature	-	350	C	(< 4 s) Note

Note: Recommended condition: 320 C max and 4 s max.

Optical and Electrical Characteristics

Since the HL1361BRxx is a bar form, the performance will depend on not only chip performance but also its assembling process including dicing. If the chip is assembled in a proper way, the performance described in Table 3 can be expected but these are not guaranteed values.

Table 3. Expected Optical and Electrical Characteristics

(Tc= -5C to 95C, unless otherwise specified, Condition at CoC (Chip on testing carrier))

No	Optical and Electrical Characteristics	Min	Typ	Max	Units	Notes
1	Wavelength range	1265 - 1340			nm	at operating output power
2	Side-mode suppression ratio (SMSR), operating condition	35	-	-	dB	
3	Threshold current @ 25C	-	8	15	mA	
4	Threshold current @ 95C	-	20	28	mA	
5	Slope efficiency @ 25C, I=Ith+5mA to I=Ith+50mA	-	0.3	-	W/A	
6	Slope efficiency @ 95C, I=Ith to I=70mA	0.11	-	-	W/A	
7	Mask Margin (IEEE 10.3Gb/s) I=Ith+25mA @25C	20	-	-	%	PRBS=2 ³¹ -1, 1k waveforms ER=4.5dB
8	Effective serial resistance I=50mA @ 95C	‘-	7	‘-	Ohms	
9	Laser forward voltage I=70mA @ 95C		1.5	2.0	V	
10	Kink deviation, Ith+5 to 100mA	-	-	20	%	See figure 6
11	Far field divergence angle, vertical, I=70mA @ 95C	-	35	45	degrees	
12	Far field divergence angle, horizontal, I=70mA @ 95C	-	32	40	degrees	

Note: Tc means sub-mount temperature when the chip mounted on Oclaro standard sub-mount soldered on a heat sink.

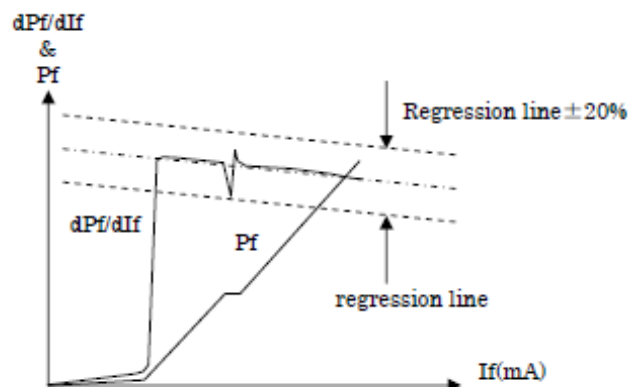


Fig. 6 Kink definition

VERIFICATION PROCESS

Oclaro will carry out the following verification test.

The bar samples will be picked up from the specified area of the finished wafer, i.e. center and middle circumferences.

- **Pulse testing:** shown in Table 4
- **Burn-in testing:** shown in Table 5 using the chips on carrier which passed the Pulse testing
- **DC testing and checking the criteria:** shown in Table 5

Table 4 Chip pulse test criteria

No.	Parameter	Symbol	Condition	Min	Max	Unit	Remark
1	Threshold current	I_{th}	$T_s=85^\circ\text{C}$	-	21.5	mA	Note1
2	Slope efficiency	Eta	$T_s=85^\circ\text{C}$, $I_F=67.5\text{mA}$	0.087	-	W/A	Note2
3	Peak wavelength	λ_p	$T_s=25^\circ\text{C}$ $I_F=67.5\text{mA}$	1288.8	1332.3	nm	
4	Side mode suppression ratio	SMSR	$T_s=25^\circ\text{C}$ $I_F=67.5\text{mA}$	35	-	dB	
			$T_s=85^\circ\text{C}$ $I_F=67.5\text{mA}$	35	-	dB	

Note1 $21.5\text{mA}=28\text{mA} \times A$, A = Temperature correlated factor 0.782

Note2 $0.087\text{W/A}=0.11\text{W/A} \times B$, B = Tester correlated factor 0.792

Wafer Verification Test

Oclaro will perform hard screening (Burn-In), DC measurement and AC measurement using chips mounted on Oclaro standard submount soldered on heat sink. Only the chips that passed the criteria described in this "Wafer Verification Test" section will be used. Only the bars from wafers meeting the minimum yield described in Table 5 will be shipped.

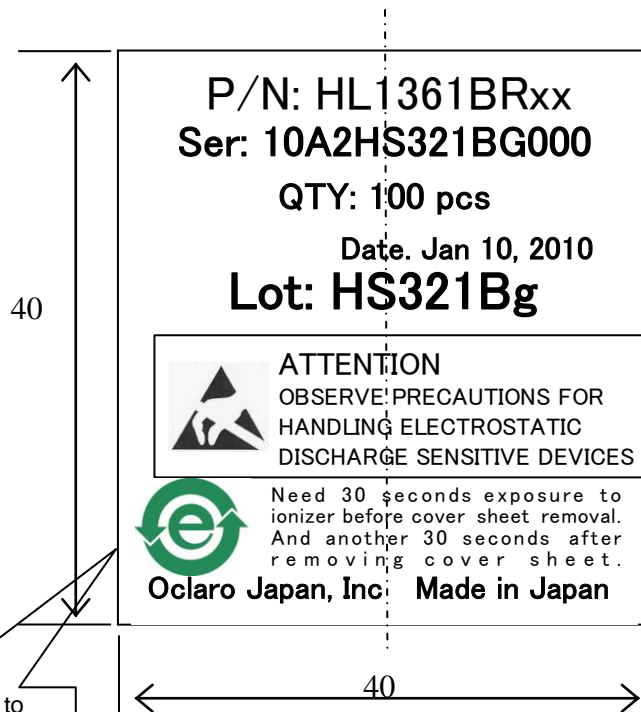
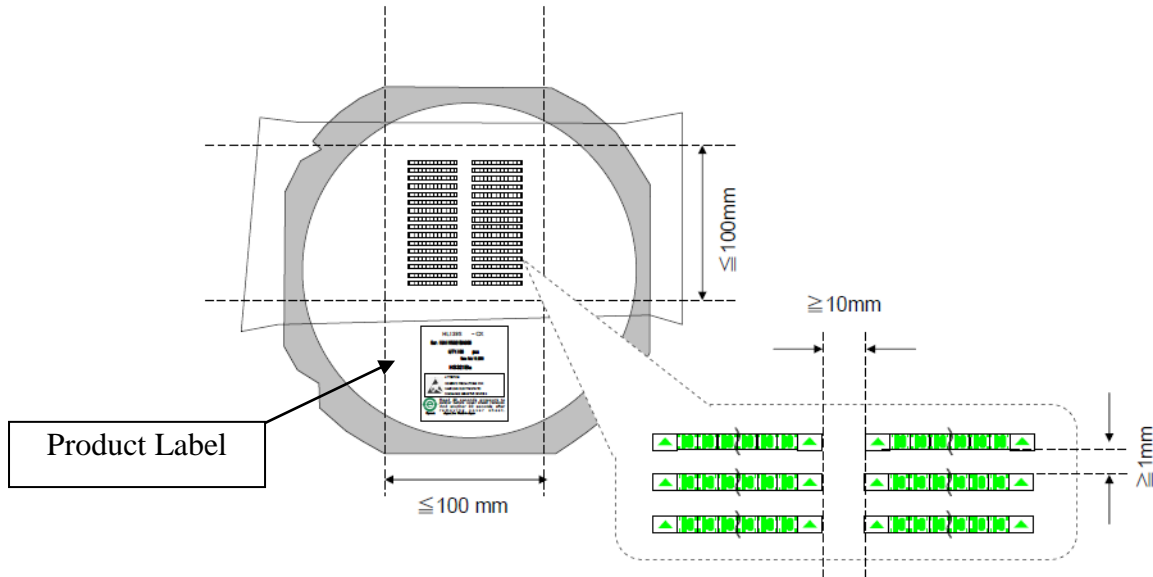
Table 5 Criteria in wafer verification test

Parameter	Condition	Pass Criterion	Minimum Number or Yield
LD chip mount	-	-	20pcs
Start Burn-In test			
Optical Purge test	25°C, 120mA, ACC 3min.	$ \Delta I_{th} \leq +5\%$, $ \Delta P_o \leq +10\%$, $ \Delta \text{Eta} \leq +10\%$.	
Electrical Purge test	100°C, 150mA, ACC 20h	-	
APC Test	95°C, 70mA, APC 100h, ($I_{op}@100h - I_{op}@0h / I_{op}@0h$)	$-2\% \leq \Delta I_{op} \leq +0.5\%$	
Pass Burn-In test			
Start DC test			
Threshold current	$T_c = 95^\circ\text{C}$	$I_{th} \leq 28\text{mA}$	
Slope efficiency	$T_c = 95^\circ\text{C}$, $\text{Eta} = P_o(70\text{mA}) / (70\text{mA} - I_{th})$	$\text{Eta} \geq 0.11\text{W/A}$	
Forward voltage	$T_c = 1^\circ\text{C}$, $I_o = 33\text{mA}$ $T_c = 95^\circ\text{C}$, $I_o = 70\text{mA}$	$V_{op} \leq 1.8\text{V}$	
Kink deviation,	$T_c = 1^\circ\text{C}$ and 95°C , $I_{th} + 5$ to 100mA	kink free	
Peak wavelength	$T_c = 1^\circ\text{C}$, $I_o = 33\text{mA}$	$1285.2\text{ nm} \leq \lambda_p \leq 1337.5\text{nm}$	
	$T_c = 95^\circ\text{C}$, $I_o = 70\text{mA}$	$1285.2\text{ nm} \leq \lambda_p \leq 1337.5\text{ nm}$	
Side mode suppression ratio	$T_c = 1^\circ\text{C}$, $I_o = 33\text{mA}$ $T_c = 95^\circ\text{C}$, $I_o = 70\text{mA}$	$\text{SMSR} \geq 35\text{dB}$	
Beam divergence angle (Horizontal)	$T_c = 95^\circ\text{C}$, $I_o = 70\text{mA}$	$\text{FWHM}_H \leq 36\text{deg}$	
Beam divergence angle (Vertical)	$T_c = 95^\circ\text{C}$, $I_o = 70\text{mA}$	$\text{FWHM}_V \leq 40\text{deg}$	
Pass DC test			10 of 20pcs (50%)

OTHER SPECIFICATIONS

Packing and label

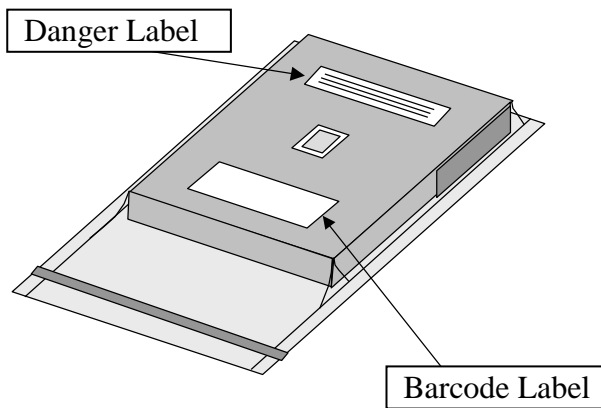
The products will be packed as described in Fig. 7 below.



This Logo is applicable to Electric Information Products (EIPs) sold within the borders of PRC (China) and to provide information as component for pollution control labeling on EIPs

Fig 7 Product label (Example)

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The plastic bag is vacuum-packed.

Fig 8 Packing bag (Example)

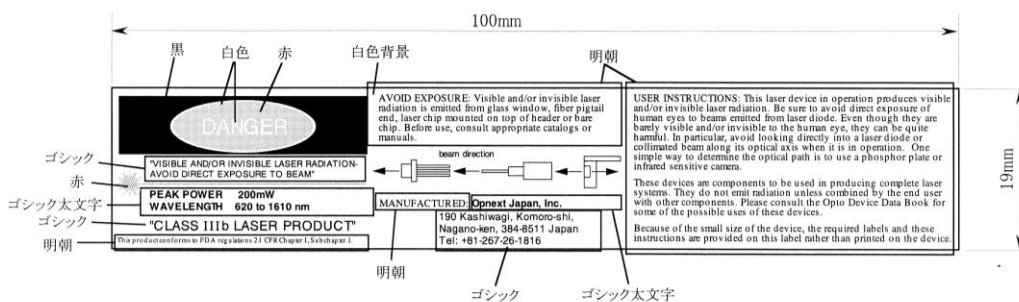


Fig 9 Danger Label (Example)

Bar code label is on plastic bag for each shipment form. Supplier Product Name, Supplier lot number, the Quantity and Customer Part Number are on it. Please see Fig.8. 40x 80 mm

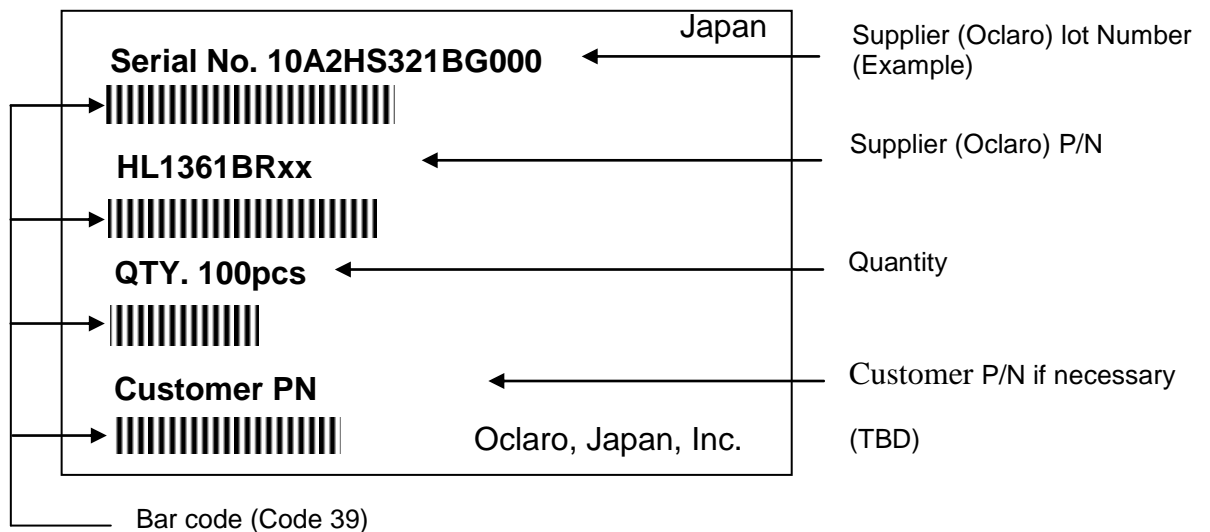


Fig. 10 Bar code label on outer plastic bag (Example of HL1361BRxx)

Revision History

Rev	Date	Page/Line/Fig/Table	Modification	Note
0.0	Aug, 04, 2014			
1.0	Dec 21, 2015	P2/	Added 35pcs bar	